Semester	III	Course Title	Computer Organization & Architecture	Course Code	18 EC 33
Teaching Period	50 Hours	L – T – P – TL*	2 – 1 – 0 – 3	Credits	3
CIE*	40 Marks	SEE*	60 Marks	Total	100 Marks

CREDITS – 03

Course Objectives: This course will enable students to:

- Explain the basic sub systems of a computer, their organization, structure and operation.
- Illustrate the concept of programs as sequences of machine instructions.
- Demonstrate different ways of communicating with I/O devices
- Describe memory hierarchy and concept of virtual memory.
- Illustrate organization of simple pipelined processor and other computing systems.

Module- 1

Basic Structure of Computers:
Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation **(up to 1.6.2 of Chap 1 of Text).**
Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(upto 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).**
L1, L2, L3

Module -2

Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions **(from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of Text).**
L1, L2, L3

Module -3

Input / Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access **(upto 4.2.4 and 4.4 except 4.4.1 of Chap 4 of Text).** **L1, L2, L3**

Module -4

Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks **(5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).** **L1, L2, L3**

Module -5

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Micro programmed Control **(up to 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).** **L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Interpret the fundamental architecture of a computer system.
- Relate and realize machine instructions and programming languages in computer architecture.
- Distinguish organize and estimate issues related to I/O units, memory units and control functions of a computer system.
- Illustrate and evaluate a CPU architecture and performance of computer system.
- Explain different ways of accessing an I/O device including interrupts.

Text Books:

- Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.

Reference Books:

- David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.
- William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.
- Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.